

# STATE ACTIVATED ONE SHOT WITH EXTENDED PULSE TIMING FOR HOT-SWAP APPLICATIONS

## 1 FIELD OF INVENTION

2 The current invention relates to the safe installation and removal of a circuit board  
3 into a system during live bus activity in the system or when installation or removal of the  
4 circuit board needs to be detected.

## 5 BACKGROUND OF THE INVENTION

6 Hot swap capability refers to the ability to insert and remove circuit boards from a  
7 system without powering down the whole system. Several hot swap schemes are  
8 disclosed in the prior art employing mechanical, electrical and electro-mechanical means  
9 to allow circuit board insertion and extraction. Many schemes use staggered pin lengths  
10 to control power connection and disconnection and circuitry to connect and disconnect  
11 output drivers from control and signal buses. By using staggered pin lengths on the hot  
12 swappable cards, the circuit can detect a hot-insertion or hot-extraction and generate a  
13 corresponding signal. In a preferred embodiment, a circuit card is employed which uses  
14 three different pin lengths. Two of the pin lengths, long and short, provide the inputs to  
15 the state activated one shot with extended pulse timing for hot-swap applications.

## 16 SUMMARY OF THE INVENTION

17 The current invention allows for the detection of a hot-insertion or a hot-extraction  
18 of a circuit board from a system by generating a signal in the form of a pulse when either  
19 occurs. In addition, the pulse remains active for a period of time after the hot-insertion or  
20 hot-extraction terminates (i.e., the circuit board is completely inserted or completely  
21 removed). This additional period of time prevents any damage or disruption of signaling  
22 caused by transient current and voltage fluctuations as the circuit board is inserted or  
23 extracted as explained below. Consequently, the state activated one-shot with extended  
24 pulse timing is ideal for bus-resets during hot-swapping.

25 Furthermore, the state activated one shot isolates power domains. This is essential  
26 during hot-swap applications to prevent latch-up and unwanted powering of a board by  
27 input signals. When a CMOS part has higher potential on its input than on its voltage  
28 supply lines, current can flow through the inputs to the CMOS power domain. When this  
29 happens, the CMOS part can go into a state known as latch-up, where it will not work  
30 properly until power cycled. This is a problem in hot-swap applications, because a circuit  
31 board being installed will not be powered up immediately, whereas its inputs can already  
32 be high.

1 In the standard case, (one of the inputs is low), the state activated one shot  
2 separates inputs and on-board power domains. This prevents the inputs from sourcing  
3 current to the on-board power domain when the on-board power is off. This is useful  
4 when the state activated one shot is itself implemented on a hot-swappable circuit board,  
5 such as in the case of redundant hot-swappable circuit boards. When said board is hot  
6 installed into the system, its on board power is initially at zero potential. If one of the  
7 inputs to the one shot is high, while the other is low (this is almost always the case), then  
8 no current will flow through Q3 (*see* Figure 1), and thus no leakage current will flow  
9 through the inputs.

10 Another advantage of the state activated one shot is that it prevents signal and data  
11 corruption. As a circuit board is inserted and removed, undesired signals such as voltage  
12 spikes can be generated on the signal lines, thereby corrupting the signals and associated  
13 data being passed through the system. The state activated one shot will prevent this  
14 corruption.

15 Finally, the state activated one shot is ideal for redundant hot-swappable circuit  
16 boards, thus eliminating the need to put circuitry on the midplane.

## 17 **BRIEF DESCRIPTION OF THE DRAWINGS**

18 Figure 1 is a logic block diagram for the State Activated One Shot with Extended  
19 Pulse Timing for Hot-Swap Applications.

20 Figure 2 is a timing diagram for the State Activated One Shot with Extended  
21 Pulse Timing for Hot-Swap Applications.

22 Figure 3 is a logic block diagram for an embodiment of the State Activated One  
23 Shot with Extended Pulse Timing for Hot-Swap Applications comprising one less  
24 Schmitt trigger inverter for inverting the output.

25 Figure 4 is a logic block diagram for an embodiment of the State Activated One  
26 Shot with Extended Pulse Timing for Hot-Swap Applications further comprising an open  
27 collector output.

28 Figure 5 is a logic block diagram for an embodiment of the State Activated One  
29 Shot with Extended Pulse Timing for Hot-Swap Applications further comprising an  
30 enable function.

31 Figure 6 is a logic block diagram for an embodiment of the State Activated One  
32 Shot with Extended Pulse Timing for Hot-Swap Applications wherein the output signal  
33 can be used in both single-ended and differential SCSI applications.

## 1 DETAILED DESCRIPTION OF THE INVENTION

2 In a preferred embodiment, the apparatus is connected to the staggered pins of a  
3 circuit board. In a board having three lengths of staggered pins, it receives as input two  
4 signals from the staggered pins. One input comes from the longest set of pins and one  
5 input comes from the shortest length set of pins. The two inputs are wired through a  
6 NAND function implemented using two Bipolar Junction Transistors or BJTs (see Fig.  
7 1). When the circuit board is completely inserted, the signal from either the longest  
8 length set of pins or the shortest length set of pins is low and the other is high. The only  
9 time both input signals are high is when the board is in transition, i.e., when the board is  
10 either being inserted or extracted from the system.

11 When both input 1 and input 2 are high (logic 1) (see time  $t_1$  on Figure 2), then  
12 neither Q1 or Q2 is biased on. (Both input 1 and input 2 are high when the board is in  
13 transition, i.e., being inserted or being extracted). Consequently, no current will flow  
14 through R3. The voltage at the collectors of Q1 and Q2 will be low or ground in this case  
15 (logic 0). This low (logic 0) will draw current from the base of Q3, causing Q3 to be  
16 biased on and causing current to flow through resistor R5. R5 will rapidly charge to  
17 voltage VDD (logic 1). This voltage is input to the Schmitt trigger inverter, S1, whose  
18 output will drop to low (logic 0). The input of inverter S2 is connected to the output of  
19 inverter S1. S2 will invert the low (logic 0) to a high (logic 1).

20 If either input 1 or input 2 goes low (logic 0) (see time  $t_2$  on Fig. 2), then the  
21 corresponding transistor (Q1 or Q2) will be biased on. Consequently, current will flow  
22 through that transistor, either Q1 or Q2, causing current to flow through R3. This will  
23 produce a voltage across R3 causing a high (logic 1) to be output at both collectors of  
24 transistors Q1 and Q2. (In fact, the only time a high (logic 1) does not appear at the  
25 output of transistors Q1 and Q2 is when both input 1 and input 2 are high. See above.  
26 Therefore, transistors Q1 and Q2 function as a NAND gate). The voltage across resistor  
27 R3 is input to the base of transistor Q3. This biases Q3 off. Consequently, no current  
28 will flow through resistor R5 which is connected to the collector of transistor Q3. The  
29 voltage across R5 will be pulled to ground. As a result, the input of inverter S1 will be  
30 pulled to ground (logic 0). Inverter S1 will invert this input to a high (logic 1). The input  
31 of inverter S2 is connected to the output of inverter S1. S2 will invert the high (logic 1)  
32 to a low (logic 0).

33 However, the output of S2 will not switch to a low (logic 0) immediately. The  
34 voltage across resistor R5, VDD, will discharge to ground voltage through the R5, C1

1 combination, where C1 is the capacitor connected between voltage VDD and the end of  
2 resistor R5 not connected to ground. Since inverter S1 is a Schmitt trigger inverter, its  
3 output will not switch to (high) logic 1, until the voltage at the input to S1 crosses a  
4 positive going threshold voltage ( $V_{T+}$ ). This will occur  $1.6 * R5 * C1$  seconds after input 1  
5 or input 2 goes low (see time  $t_3$  on Figure 2). Inverter S2 inverts this low (logic 0) to a  
6 high (logic 1). Therefore, the RC combination acts to extend the time duration of the  
7 pulse at the output of inverter S2. It effectively acts as a time extender circuit.  
8 Consequently, the output pulse from inverter S2 remains asserted during the period of  
9 time when one or both inputs are logic 1 and for a time period after one of the inputs goes  
10 to logic 0, determined by the equation  $1.6 * R5 * C1$ .

11 In a second embodiment, the second Schmitt trigger inverter, S2, can be removed  
12 if opposite polarity is required (see Figure 3).

13 In still another embodiment, a series resistor, R6, connected to the base of a  
14 transistor, Q4, can be added if an open collector output is required, such as for Single-  
15 Ended SCSI applications (a SCSI bus reset during a hot-swap, for instance) (see Figure  
16 4).

17 In still another embodiment, an enable can be added to the state activated one-shot  
18 by attaching a NPN transistor, Q5, to the output of inverter S2 (See Figure 5). The input  
19 of Q5 receives as input an enable signal, OUTPUT\_ENABLE. In the case where  
20 OUTPUT\_ENABLE is low, Q5 turns off and no current flows through Q5.  
21 Consequently, the output of inverter S2 is unaffected. On the other hand, when  
22 OUTPUT\_ENABLE signal is high, Q5 turns on, thereby conducting current through  
23 resistor R6. Thus, Q5 acts like a current sink pulling current from the output of inverter  
24 S2. This drives the input of inverter S2 low (logic 0), thereby disabling the state activated  
25 one-shot.

26 Figure 6 shows an embodiment of the state activated one shot which enables its  
27 use with differential SCSI applications. In this application, the output of Schmitt trigger  
28 S2 is input to one input of a two input NAND gate U2 and, also, to the input of a  
29 transistor Q7. In addition, two comparators, U1-A and U1-B, are connected to provide  
30 complementary outputs. The output of the first comparator, U1-A, is input to the second  
31 input of NAND gate U2, while the output of the second comparator, U1-B, is input to  
32 transistor Q8. Resistors R8 and R9 act as a voltage divider, thereby setting a threshold  
33 voltage,  $(VDD * R9) / (R8 + R9)$ , for the complementary comparators, U1-A and U1-B. (In  
34 a preferred embodiment, the threshold is set at 0.7 Volts).

1       When differential outputs are desired, signal 1DIFFSENS goes HIGH. (In a  
2 preferred embodiment, 1DIFFSENS goes greater than 0.7 Volts). This causes the output  
3 of comparator U1-A to go logic HIGH. This will cause the NAND gate to track the  
4 output of Schmitt trigger, S2. For example, when the output of S2 is logic HIGH, the  
5 output of NAND gate U2 is low. Consequently, pnp transistor Q6 will be biased on and it  
6 will source current onto line 1RST+. On the other hand, when the output of S2 is logic  
7 LOW, the output of NAND gate U2 will go HIGH. Consequently, pnp transistor Q6 will  
8 be biased off, and no current will be sourced.

9       In addition, when signal 1DIFFSENS goes HIGH, the output of comparator U1-B  
10 will go logic LOW. This turns npn transistor Q8 off. As a result, current will flow  
11 through resistor R10. Also, transistor Q7 will track the output of Schmitt trigger S2. For  
12 example, when the output of S2 is logic HIGH, npn transistor Q7 will be biased on and  
13 act as a current sink, sinking current on line 1RST-. On the other hand, when the output  
14 of S2 is logic LOW, npn transistor Q7 will be biased off. Consequently, it won't sink  
15 current.

16       If operation in single ended mode is desired, signal 1DIFFSENS goes  
17 LOW. (In a preferred embodiment, 1DIFFSENS goes less than 0.7 Volts). This  
18 causes the output of comparator U1-A to go logic LOW. This will cause the output of  
19 NAND gate U2 to always remain at logic HIGH. Consequently, pnp transistor Q6 will  
20 always be biased off and no current will be sourced onto line 1RST+.

21       In addition, when signal 1DIFFSENS goes LOW, the output of comparator U1-B  
22 will go logic HIGH. This turns npn transistor Q8 on. Consequently, current will flow  
23 through transistor Q8, and not resistor R10. Transistor Q7 will still track the output of  
24 Schmitt trigger S2. For example, when the output of S2 is logic HIGH, npn transistor Q7  
25 will be biased on and act as a current sink, sinking current on line 1RST-. However, in  
26 this case (single-ended mode), the current will be sunk to ground, as opposed to being  
27 sunk through a resistor to ground (differential mode). When the output of S2 is logic  
28 LOW, npn transistor Q7 will be biased off. Consequently, it won't sink current. In a  
29 preferred embodiment, a switching apparatus can be substituted for transistor Q8.

30       While the invention has been disclosed in this patent application by reference to  
31 the details of preferred embodiments of the invention, it is to be understood that the  
32 disclosure is intended in an illustrative rather than in a limiting sense, as it is  
33 contemplated that modifications will readily occur to those skilled in the art, within the  
34 spirit of the invention and the scope of the appended claims.